AMENDMENTS TO THE CLAIMS

Claims 1-13 (Cancelled)

14. (Currently Amended) A method of forming a semiconductor device, the method comprising:

~~forming a layer of insulation material over a semiconductor substrate;~~

forming a layer of conductive material on ~~the~~ a conductive region and a layer of insulation material;

etching the layer of conductive material to form a trace, the trace having a first length, a first width, a first height, a top surface and a bottom surface;

etching the trace to form a ~~number of slot openings~~ slot opening in the top surface of the trace, the slot ~~openings each~~ opening having a bottom surface spaced apart from the bottom surface of the trace, a second length, a second width, and a second height, the first and second lengths being substantially equal; and

forming a layer of isolation material over the trace to fill up the slot ~~openings~~ opening.

15. (Original) The method of claim 14 wherein the trace is formed to have a number of loops.

16. (Original) The method of claim 15 wherein the loops lie substantially in a same plane.

17. (Original) The method of claim 14 wherein the trace is connected to a contact.

18. (Original) The method of claim 14 wherein the trace is connected to a via.

19. (Previously Presented) The method of claim 14 wherein the layer of isolation material contacts the layer of insulation material.

20. (Previously Presented) The method of claim 14 wherein the conductive material is metal.

Claims 21-22 (Cancelled)

23. (New) A method of forming a semiconductor device, the method comprising:

forming a layer of conductive material on a conductive region and a layer of insulation material;

etching the layer of conductive material to form a trace, the trace having a length, a width, a height, a top surface, and a bottom surface;

etching the trace to form a slot opening in the top surface of the trace, the slot opening having a bottom surface spaced apart from the bottom surface of the trace, and side walls that extend along the length of the trace; and

forming a layer of isolation material over the trace to fill up the slot openings.

24. (New) The method of claim 23 wherein the trace is formed to have a number of loops.

25. (New) The method of claim 24 wherein the loops lie substantially in a same plane.

26. (New) The method of claim 23 wherein the layer of isolation material contacts the layer of insulation material.

27. (New) The method of claim 23 wherein the conductive material is metal.

28. (New) The method of claim 23 wherein the slots are substantially equally spaced apart.

29. (New) A method of forming a semiconductor device, the method comprising:

forming a layer of conductive material on a conductive region and a layer of insulation material;

etching the layer of conductive material to form a trace, the trace having a bottom surface and a substantially planar top surface;

etching the trace to form a plurality of slot openings in the top surface of the trace, each slot opening having a bottom surface spaced apart from the bottom surface of the trace, a portion of each slot opening lying directly vertically over the conductive region; and

forming a layer of isolation material over the trace to fill up the slot openings.

30. (New) The method of claim 29 wherein the trace is formed to have a number of loops.

31. (New) The method of claim 30 wherein the loops lie substantially in a same plane.

32. (New) The method of claim 29 wherein the metal region is a via.

33. (New) The method of claim 29 wherein the layer of isolation material contacts the layer of insulation material.

34. (New) The method of claim 29 wherein the conductive material is metal.

35. (New) The method of claim 29 wherein the slots are substantially equally spaced apart.